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REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 1-8 and 11-15 are pending in this application. Claim 1 and claim 11 are amended herein. Claims 9-10 are canceled herein. Claims 14-15 are newly added herein. No claims have been allowed.

The amendments to applicant's specification are provided to address typographic errors and omissions therein.

Claim Rejections - 35 U.S.C. §§ 102 and 103

1. The Examiner has rejected claims 1, 3-6, 8-10 and 12-13 under 35 U.S.C. § 102(e) as being anticipated by Kelly et al. (U.S. Patent No. 6,143,117; hereinafter "Kelly").

2. The Examiner has rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Kelly.

3. The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Davidson (U.S. Patent No. 5,880,010).

4. The Examiner has rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Sato et al. (U.S. Patent No. 6,309,945; hereinafter "Sato").

Applicant acknowledges the teachings of Kelly and Davidson as cited by the Examiner, but not the teachings of Sato as cited by the Examiner.

With respect to Sato, applicant asserts that Sato at col. 7, lines 56-65 does not (as cited by the Examiner) disclose a chemical mechanical polish (CMP) planarizing method for removing from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication a second substrate in accord with applicant's invention as disclosed and claimed with respect to applicant's claim 11 (and related base and intervening claims), but rather Sato clearly discloses at col. 7, lines 56-65 an etch method for removing Sato's porous silicon layer from Sato's laminated microelectronic fabrication.

Applicant has in addition amended applicant's claim 1 to incorporate therein limitations of applicant's claim 9, claim 10 and claim 11, while canceling claim 9 and claim 10, and amending claim 11 accordingly, to provide within amended claim 1 second substrate removal methodologic limitations which applicant asserts are not disclosed within Kelly, Davidson, Sato or any combination thereof.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within amended claim 1 is not disclosed within Kelly, Davidson, Sato or any combination thereof, particularly with respect to specifically enumerated removal methods for removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication in accord with applicant's invention, applicant asserts that

amended claim 1 may not properly be rejected under 35 U.S.C. § 103(a) over any combination of references derived from Kelly, Davidson or Sato.

Since all remaining claims within this application are dependent upon amended claim 1 and carry all of the limitations of amended claim 1, applicant additional asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) over any combination of references derived from Kelly, Davidson and Sato.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of: (1) claims 1, 3-6, 8-10 and 12-13 under 35 U.S.C. § 102(e) as being anticipated by Kelly; (2) claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Kelly; (3) claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Davidson; and (4) claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Sato, be withdrawn.

Other Considerations

Applicant has newly added claims 14 and 15 as directed towards a compression laminating method for laminating applicant's partially fabricated semiconductor integrated circuit microelectronic fabrication and applicant's dielectric isolated metallization pattern, wherein the compression laminating method employs an indium or indium alloy compression bonding material. Support for newly added claims 14 and 15 is found within claim 1, claim 8 and applicant's specification within the paragraph bridging pages 12-13

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The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention.

No fee is due as a result of this Amendment and Response.

SUMMARY

Applicant's invention as disclosed and claimed within amended claim 1 provides a laminating method for forming a microelectronic fabrication. The laminating method laminates a partially fabricated semiconductor integrated circuit microelectronic fabrication with a dielectric isolated metallization pattern formed in inverted order over a second substrate. The second substrate is then removed employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods. Applicant's invention as disclosed and claimed within claim 14 provides that applicant's partially fabricated semiconductor integrated circuit microelectronic fabrication and applicant's inverted dielectric isolated metallization pattern are laminated employing a pressure laminating method. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within amended claim 1 and claim 14.

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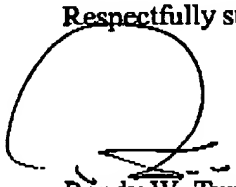
CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,



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APPENDIX I

PORTIONS OF THE SPECIFICATION

(MARKED-UP WITH CURRENT REVISIONS)

Paragraph bridging pages 12-13.

Finally, within the preferred embodiment of the present invention with respect to the pair of conductor contact studs 22a and 22b, the pair of conductor contact studs 22a and 22b may be formed of conductor materials as are conventional in the art of microelectronic fabrication, including but not limited to metal, metal alloy, doped polysilicon and polycide conductor stud materials. However, as is understood by a person skilled in the art, it is preferred within the context of the present invention that the pair of conductor contact studs 22a and 22b is formed of a conductor material, and of dimensions, such as to facilitate within the context of the present invention bonding of the pair of conductor contact studs 22a and 22b with a pair of patterned conductor layers within a dielectric isolated metallization pattern subsequently laminated thereto. Thus, at least an upper portion of the conductor contact studs 22a and 22b may be formed of a thermally bondable metal (i.e., a solder) or a pressure bondable metal (for example and without limitation an indium or an indium alloy pressure bondable material), or may protrude from above the plane of the patterned planarized pre-metal dielectric layers 20a, 20b and 20c in order to facilitate bonding.

Page 14, first paragraph.

Finally, with respect to the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1, as is understood by a person skilled in the art, the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 is illustrated as a partially fabricated semiconductor integrated circuit microelectronic fabrication 24, insofar as it is desirable to fabricate upon the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 a dielectric isolated metallization pattern at least in part to provide a completely fabricated semiconductor [fabricated semiconductor] integrated circuit microelectronic fabrication.

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APPENDIX II

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. (amended) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication; [and]

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods.

2. The method of claim 1 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. The method of claim 1 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. The method of claim 1 wherein the second substrate is a second semiconductor substrate.

5. The method of claim 1 wherein the first semiconductor substrate is thicker than the second substrate.

6. The method of claim 1 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

7. The method of claim 6 wherein each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3000 to about 6000 angstroms.

8. The method of claim 1 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

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9. - 10. (canceled)

11. (amended) The method of claim [9] 1 wherein the [second substrate is removed from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication employing a] chemical mechanical polish (CMP) planarizing method [while employing] employs the dielectric isolated metallization pattern as a[n etch] stop layer.

12. The method of claim 1 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. The method of claim 1 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

14. (newly added) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication; and

pressure laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a pressure laminated completely fabricated semiconductor integrated circuit microelectronic fabrication.

15. (newly added) The method of claim 14 wherein the partially fabricated semiconductor integrated circuit microelectronic fabrication and the second substrate are pressure laminated while employing a bonding material selected from the group consisting of indium and indium alloy bonding materials.